

MMQ65R026S6FZ

650V 0.026Ω N-channel MOSFET

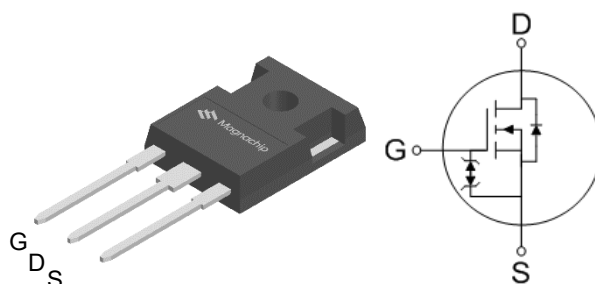
Description

Superior 6th generation Fast Recovery SJ MOSFETs (S6F series) are cutting-edge high voltage power MOSFETs, based on Magnachip's extensive design expertise and years of experience. The S6F series, featuring an ultra-fast body diode, show excellent performance with very low reverse recovery charge (Q_{rr}) and time (t_{rr}). As a result, it offers better performance in bridge and ZVS topologies. Moreover, these user friendly devices offer the advantages of improved ruggedness, making it an ideal choice for designers.

Key parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	0.026	Ω
$V_{TH,typ}$	4.0	V
I_D	101	A
$Q_{g,typ}$	180	nC

Package & internal circuit



Features

- Ultra-fast body diode
- Low power loss by high speed switching and low on-resistance
- 100% avalanche tested
- Green package – Pb free plating, halogen free
- Zener-integrated

Applications

- Soft-switching applications
- Server power supply
- Uninterruptible power supply (UPS)
- EV charging

Ordering Information

Order Code	Marking	Temp. Range	Package	Packing	RoHS Status
MMQ65R026S6FZTH	65R026S6FZ	-55 ~ 150°C	TO-247	Tube	Compliant

■ Absolute maximum rating ($T_c=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit	Note
Drain-source voltage	V_{DSS}	650	V	
Gate-source voltage	V_{GSS}	± 25	V	
Continuous drain current ¹⁾	I_{D}	101	A	$T_c=25^{\circ}\text{C}$
		64	A	$T_c=100^{\circ}\text{C}$
Pulsed drain current ²⁾	I_{DM}	303	A	
Power dissipation	P_{D}	291	W	
Single-pulse avalanche energy ³⁾	E_{AS}	406	mJ	
MOSFET dv/dt ruggedness	dv/dt	120	V/ns	
Continuous diode forward current	I_{SD}	101	A	
Diode dv/dt ruggedness ⁴⁾	dv/dt	50	V/ns	
Storage temperature	T_{stg}	-55 ~150	$^{\circ}\text{C}$	
Maximum operating junction temperature	T_{j}	150	$^{\circ}\text{C}$	

1) I_{D} limited by maximum junction temperature, Duty cycle $D=0.5$

2) Pulse width t_{p} limited by $T_{\text{j,max}}$

3) $I_{\text{AS}} = 10.7 \text{ A}$

4) $I_{\text{SD}} \leq I_{\text{D}}$, $V_{\text{DS peak}} \leq 400\text{V}$, $di/dt \leq 900\text{A}/\mu\text{s}$

■ Thermal characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case max	R_{thJC}	0.38	$^{\circ}\text{C}/\text{W}$
Thermal resistance, junction-ambient max	R_{thJA}	62.5	$^{\circ}\text{C}/\text{W}$

■ Static characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain–source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS} = 0V, I_D = 1mA$
Gate threshold voltage	$V_{GS(th)}$	3.0	4.0	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	17	μA	$V_{DS} = 650V, V_{GS} = 0V$
Gate leakage current	I_{GSS}	-	-	10	μA	$V_{GS} = \pm 25V, V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(ON)}$	-	0.023	0.026	Ω	$V_{GS} = 10V, I_D = 42A$

■ Dynamic characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input capacitance	C_{iss}	-	10800	-	pF	$V_{DS} = 400V, V_{GS} = 0V, f = 250kHz$
Output capacitance	C_{oss}	-	181	-		
Reverse transfer capacitance	C_{rss}	-	14	-		
Effective output capacitance energy related ⁵⁾	$C_{o(er)}$	-	287	-		$V_{DS} = 0V \text{ to } 400V, V_{GS} = 0V, f = 250kHz$
Effective output capacitance time related ⁶⁾	$C_{o(tr)}$	-	2005	-		$V_{DS} = 0V \text{ to } 400V, V_{GS} = 0V, f = 250kHz$
Turn-on delay time	$t_{d(on)}$	-	217	-	ns	$V_{GS} = 10V, R_G = 25\Omega, V_{DD} = 325V, I_D = 101A$
Rise time	t_r	-	201	-		
Turn-off delay time	$t_{d(off)}$	-	414	-		
Fall time	t_f	-	73	-		
Total gate charge	Q_g	-	180	-	nC	$V_{GS} = 10V, V_{DD} = 400V, I_D = 42A$
Gate–source charge	Q_{gs}	-	67	-		
Gate–drain charge	Q_{gd}	-	54	-		
Gate resistance	R_G	-	2.1	-	Ω	$V_{GS} = 0V, f = 1MHz$

5) $C_{o(er)}$ is a capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

6) $C_{o(tr)}$ is a capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

■ Reverse diode characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Diode forward voltage	V_{SD}	-	-	1.4	V	$I_{SD} = 42\text{A}$, $V_{GS} = 0\text{V}$
Reverse recovery time	t_{rr}	-	292	-	ns	$I_{SD} = 42\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 400\text{V}$
Reverse recovery charge	Q_{rr}	-	6.7	-	μC	
Reverse recovery current	I_{rm}	-	23	-	A	

■ Characteristic graph

Fig.1 On-region characteristics.

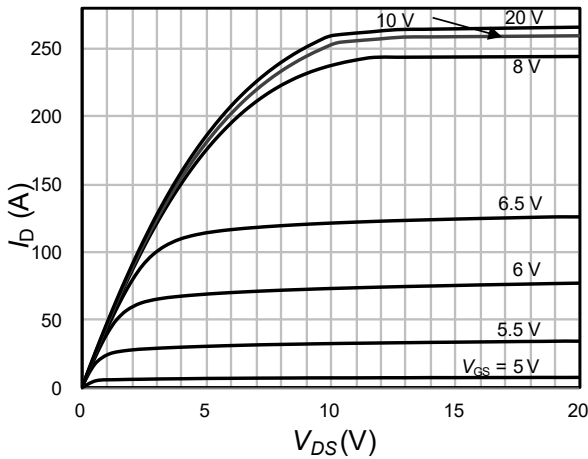


Fig.2 On-resistance variation with drain current

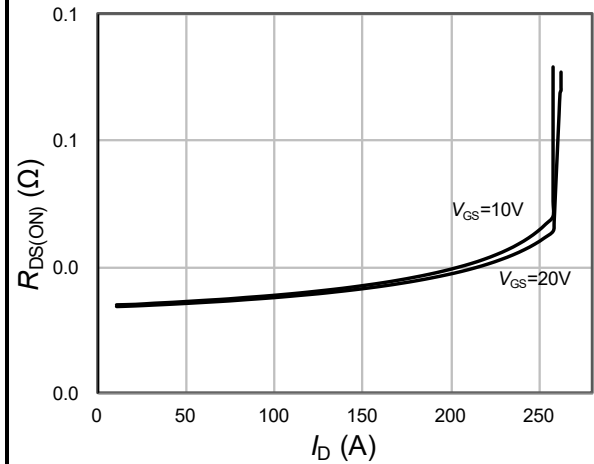


Fig.3 On-resistance variation with junction temperature (normalized)

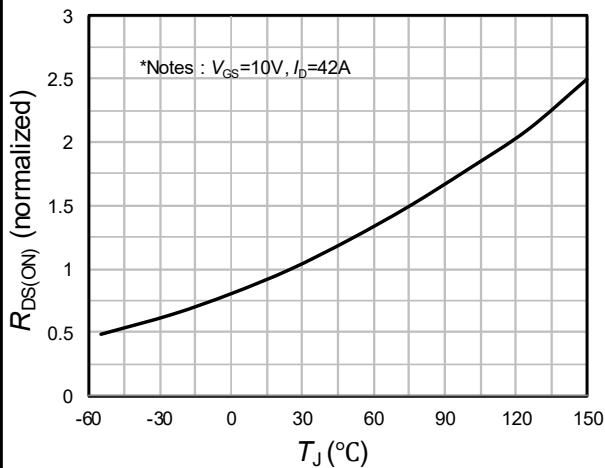


Fig.4 Breakdown voltage variation with temperature (normalized)

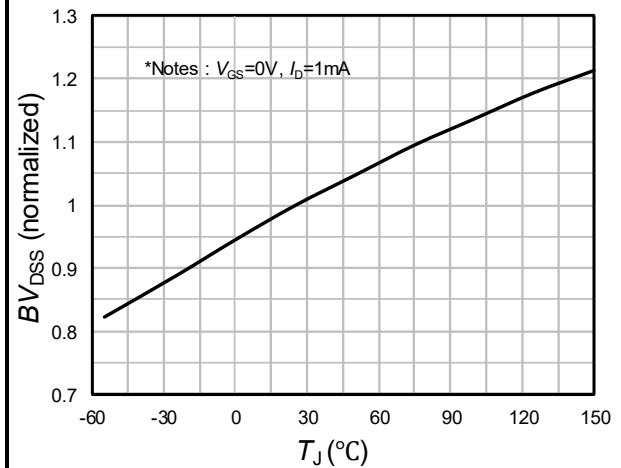


Fig.5 Transfer characteristics

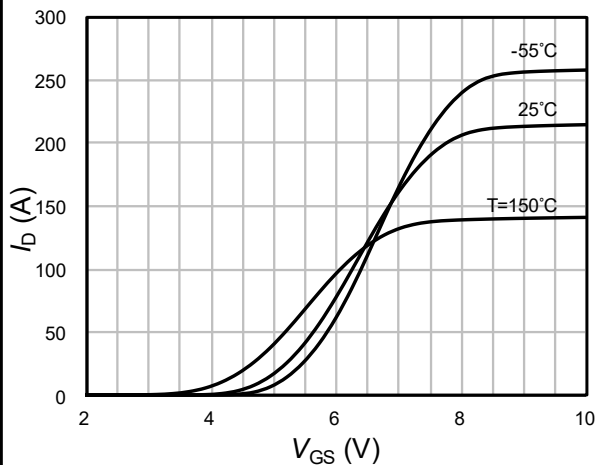


Fig.6 Diode forward characteristics

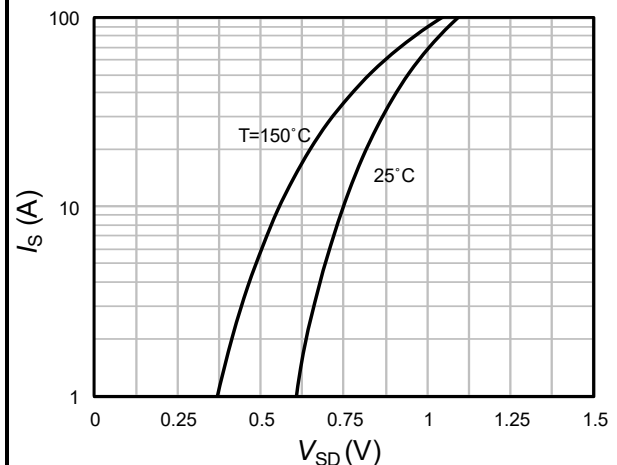


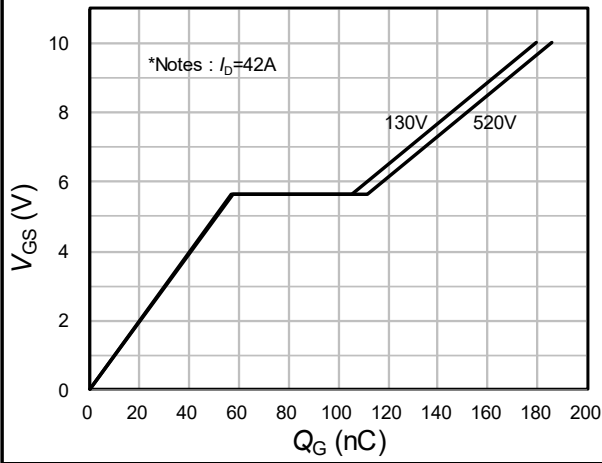
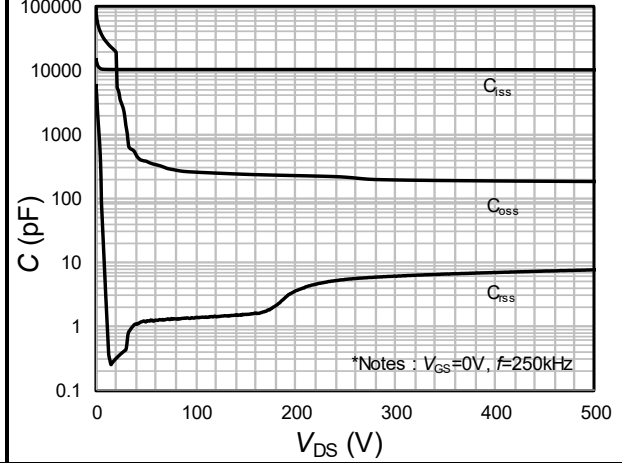
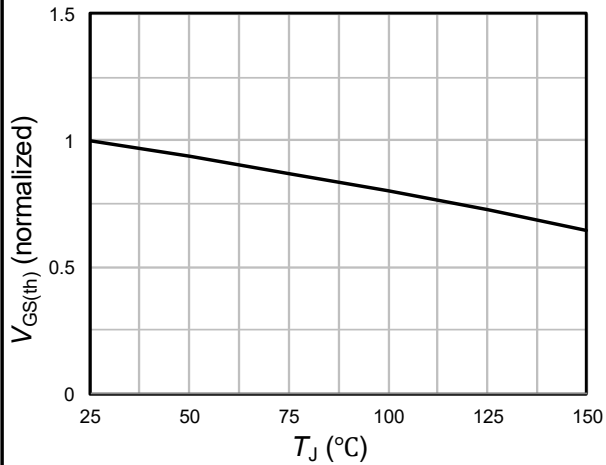
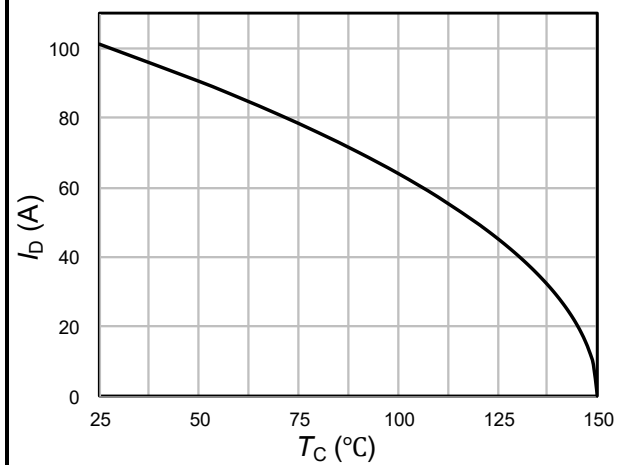
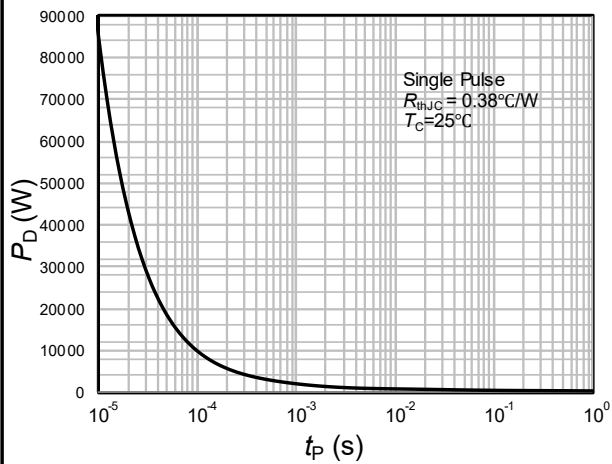
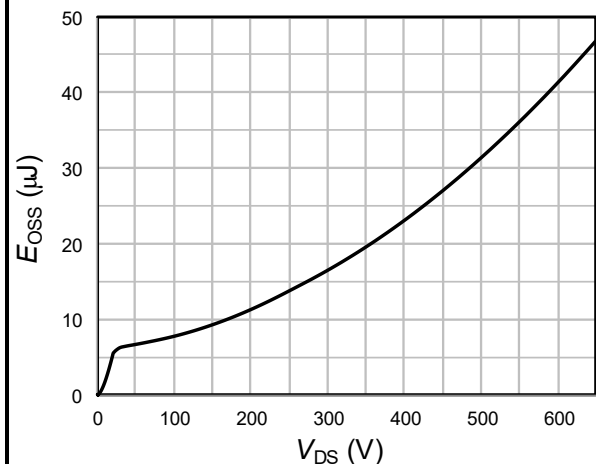
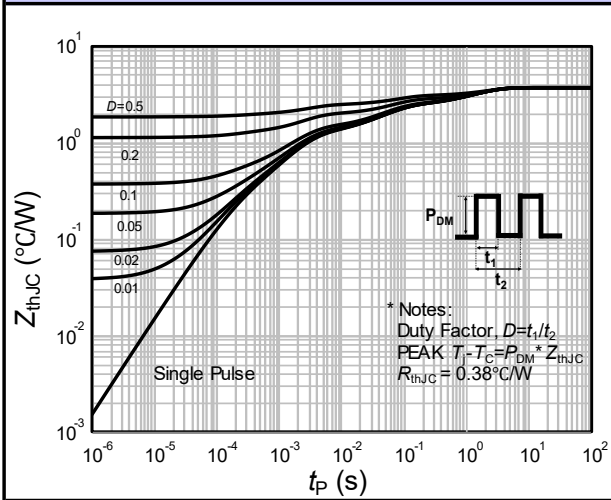
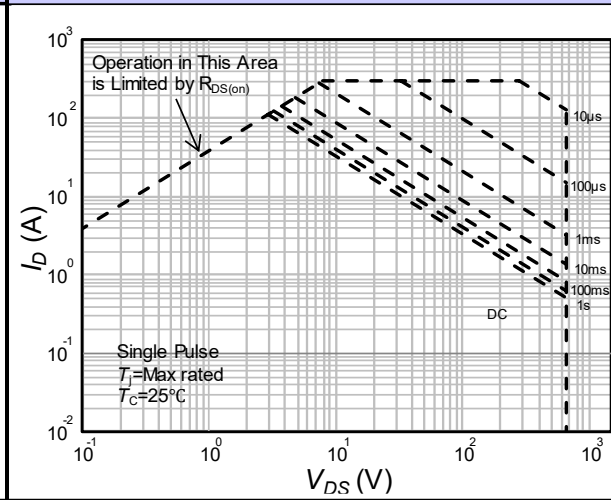
Fig.7 Gate charge characteristics

Fig.8 Capacitance characteristics

Fig.9 Threshold voltage variation with junction temperature

Fig.10 Drain current

Fig.11 Power dissipation variation with pulse time

Fig.12 Output capacitance stored energy


Fig.13 Transient thermal response

Fig.14 Safe operating area


The graph shows the relationship between gate voltage V_{GS} and charge. The solid line represents the gate voltage profile during a switching event. It starts at the origin, rises linearly to the threshold voltage (indicated by a dashed line at 10V), remains constant at 10V for a short duration, and then rises linearly again. The total gate charge Q_g is the area under this curve. The gate-to-source charge Q_{gs} is the charge required to raise the gate voltage from 0V to 10V. The gate-to-drain charge Q_{gd} is the charge required to keep the gate voltage at 10V while the drain voltage falls.

[illegible]

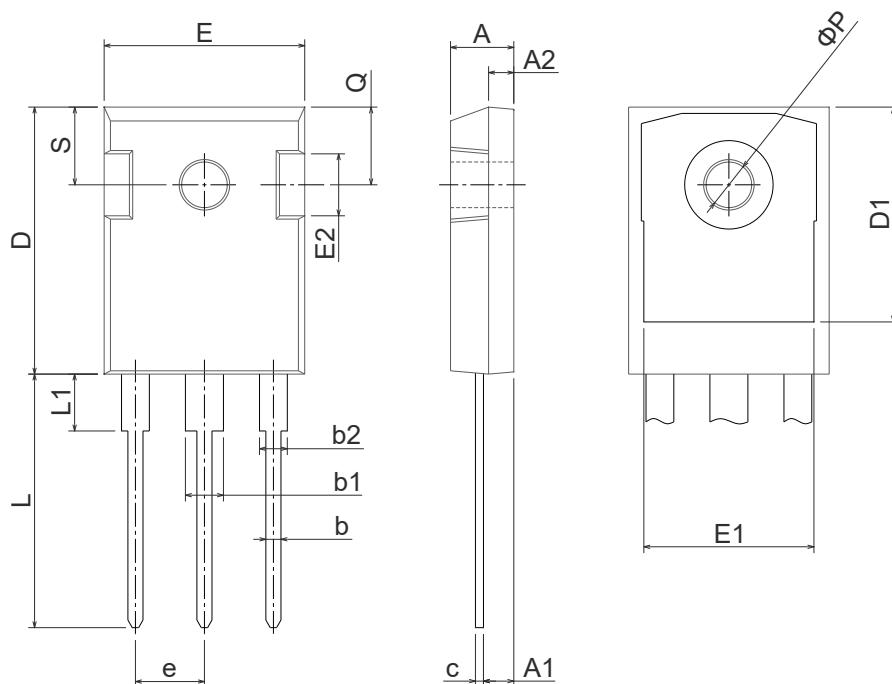
The diagram shows a common-source amplifier circuit. The input gate voltage V_{gs} is applied through a gate resistor R_g to the gate of the DUT. The drain of the DUT is connected to a load inductor L and a current source I_{AS} . The output voltage V_{DS} is taken from the drain. A DC bias voltage V_{DD} is applied to the drain through a coupling capacitor.

[illegible]

Physical dimension

TO-247

Dimensions are in millimeters, unless otherwise specified



Dimension	Min(mm)	Max(mm)
A	4.70	5.31
A1	2.20	2.60
A2	1.50	2.49
b	0.99	1.40
b1	2.59	3.43
b2	1.65	2.39
c	0.38	0.89
D	20.30	21.46
D1	13.08	-
E	15.45	16.26
E1	13.06	14.02
E2	4.32	5.49
e	5.45BSC	
L	19.81	20.57
L1	-	4.50
ΦP	3.50	3.70
Q	5.38	6.20
S	6.15BSC	

DISCLAIMER:

The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.

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